10 AND 26 GHz DIFFERENTIAL VCOs USING InP HBTs

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ABSTRACT

We have built 10 and 26 GHz differential VCOs using InP HBTs. Both oscillators use a 3 stage emitter coupled pair ring section. The 10 GHz VCO is connected in the well known fashion but the 26 GHz circuit uses a patented [1] summed output from each of the three ECP (Emitter Coupled Pair) stages. The circuits are powered from a single 5V supply consuming 250 mW. The chip size is 870X975 μm^2. The phase noise at a 100 kHz offset for the 10 and 26 GHz oscillators is -83 dBc/Hz and -70 dBc/Hz respectively.

INTRODUCTION

As the spectrum at low gigahertz frequencies becomes saturated with applications, the demand to move to higher frequencies will increase. There is already substantial spectrum available at 28 and 38 GHz, which is stimulating interest at those frequencies. A key element of any wireless design is the generator or oscillator. A number of high performance oscillators have been demonstrated using HBT technology [2-7]. The designs referenced here have lower phase noise due to using one or two transistor designs. Our designs provide differential outputs and use up to 40 HBTs. One of the highest frequency VCO circuits use GaAs P-HFET technology achieving 75.2 GHz operation with an estimated phase noise of -80 dBc/Hz and an output power of 8mW [8]. Tuning range is another important parameter and a Si BJT design having a 20 GHz range with center frequency of 22 GHz has been demonstrated [9]. Finally, a 4 stage ring oscillator was simulated using GaAs HBT parameters to give 5 GHz performance [10].

In this paper we describe two InP HBT ring oscillators. The basic design is built using three stages to generate a 3 gate delay circuit. The second design builds upon the basic design by summing the output from each of the basic designs three stages. To the best of our knowledge the performance presented here demonstrates the highest frequency differential ring oscillator reported to date.

TH 3B

DEVICE TECHNOLOGY

The HBTs were grown using MOMBE. The device structure shown in table 1, consists of a 0.4μm subcollector, 2E19cm^{-3} followed

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by a composite collector of 0.55μm InP and two GaInAsP quaternary step graded layers each 0.015μm, all at 2E16cm^{-3}. The base

Material	Thickness (nm)	Type	Dopant	Level (cm^{-3})
GaInAs	100	n+	Sn	3X10^{19}
InP	100	n	Sn	5X10^{18}
InP	100	n	Sn	5X10^{17}
GaInAs	2	n-	Sn	1X10^{16}
GaInAs	70	p+	C	3X10^{19}
GaInAs	50	n-	Sn	1X10^{16}
GaInAsP	15, Q=1.3	n-	Sn	2X10^{16}
GaInAsP	15, Q=1.1	n-	Sn	2X10^{16}
InP	550	n-	Sn	2X10^{16}
GaInAs	20	n	Sn	1X10^{18}
GaInAs	400	n+	Sn	2X10^{19}
InP Fe Doped Substrate				

Table 1: InP HBT layer structure.

was GaInAs 0.07μm Carbon doped at 3E19cm^{-3}. The two InP emitter layers were each 0.1μm have impurity levels of 5E17cm^{-3} and 5E18cm^{-3}. Finally to insure a good emitter contact, a 0.1μm GaInAs cap at 3E19cm^{-3} was included.

The HBT performance was measured on a 3X5μm^2 device at I_C=3.2 mA and V_{CE}=2.5 V. The f_T and F_{max} for the bias conditions were 53 GHz and 45 GHz respectively. The dc current gain β was 66 for I_C=3.2 mA and V_{CE}=2.5 V.

CIRCUIT DESCRIPTION

The block diagram of the 26 GHz summed output oscillator is shown in figure 1. Each ECP block contains a differential pair, active current sources, and output emitter followers. Three such stages form the basic core for the oscillator. After each stage a sample of the output voltage is taken by adding an additional emitter coupled pair in parallel with the input to the next stage. The collectors of the sampling pairs are connected together at a common resistive load. This load and the three sampling emitter coupled pairs form the sum block in the diagram. The voltage generated across the common load is the desired output voltage V_{out}. This output is the sum of the output of each ring stage V1, V2, and V3. The summed oscillator timing diagram is shown in figure 2. If the ECP stage delay is τ, then the round trip time through the circuit should have period 3τ. The voltages V1, V2, and V3 should be exactly the same and delayed by τ from each other. If all of the stages are identical then |V1|=|V2|=|V3|, and the first point for V_{out} is obtained by adding the three voltages and is found to be V+V-V, or just V. Every τ/2 there is a transition and hence the period of V_{out} is simply τ. The time τ is related to the transit time of the transistor as in the case for a standard ring oscillator. Thus ideally, a single transistor delay should be obtained for this oscillator. The frequency of this oscillator can be changed by changing the current in each ECP stage. There are setup

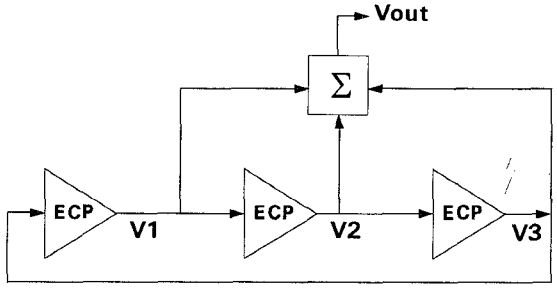

Figure 1: 26 GHz oscillator block diagram.

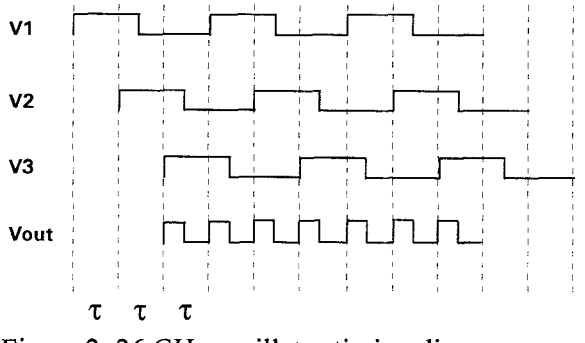

Figure 2: 26 GHz oscillator timing diagram.

resistors to the V_{CC} supply and the point at which each connect to the current mirror is brought out to a bond pad. Applying a voltage to the common current mirror bias point changes the current in each ECP and hence the delay through it, this then changes the frequency of the oscillator. In addition, the circuits can also be operated as current controlled oscillators by injecting additional current into the bias set-up leg of the current mirrors.

MEASURED RESULTS

Figure 3 is the measured output spectrum for the differential summed output oscillator.

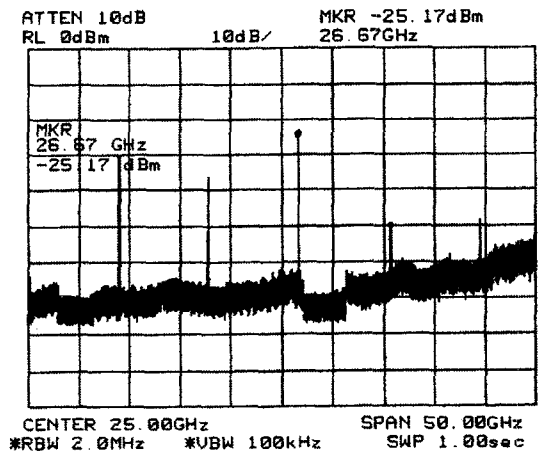

Figure 3: 26 GHz oscillator output spectrum.

The largest spur occurs at a frequency of 26.67 GHz. For comparison, the standard 3 stage ring oscillator had a measured frequency of 9.67 GHz. The frequency of the oscillator should have been 29 GHz by comparison. The difference occurs due to the additional parasitic of the sampling ECPs loading down the oscillator. Referring again to figure 3 the lowest frequency spur is that of the fundamental ring core and is at 8.89 GHz (compared to 9.67 GHz of the standard design). The spur at 17.78 GHz is the second harmonic of the core oscillator. Note that the 3rd harmonic of the core appears at the same frequency as the summed oscillator. Since the design is differential, the even harmonics that occur should by design be attenuated lower than that of a single ended architecture. The single ended design however was not built on the same wafer for comparison.

The phase noise of the oscillator was also measured using the HP8565E spectrum analyzer and is shown in figure 4. The graph shows the phase noise in dBc/Hz. The marker at the spot frequency of 100 kHz has a value of -77 dBc/Hz. Even though

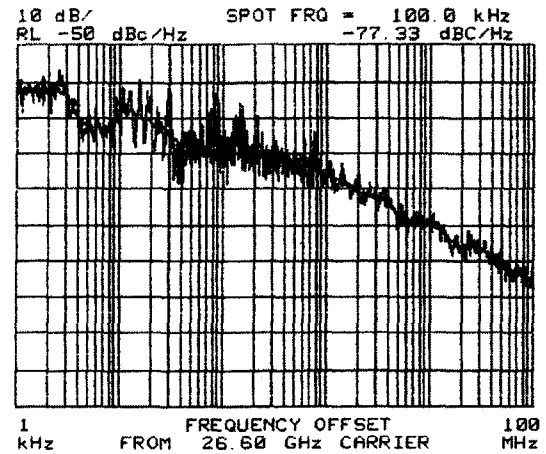

Figure 4: 26 GHz oscillator output phase noise.

measurements were made from 1 kHz to 100 MHz, the lower frequencies have significant error due to the increased amount of phase noise in the oscillator. Below about 300 kHz, the linear extrapolation from higher frequencies gives about -70 dBc/Hz at 100 kHz. At 1 MHz the phase noise was measured to be -85 dBc/Hz. This curve illustrates that this multi-transistor design has a larger phase noise when compared to other single transistor oscillators [2-9].

Finally, figure 5 shows the circuit layout for the 26 GHz oscillator. The design has exact symmetry along the V_{CC} axis through the middle of the chip eliminating any offsets that may occur at this frequency due to line

length mismatches. The metallization used was electrodeposited gold 1 μm thick. The resistors used were NiCr and had a sheet resistance of 25 Ω/sq. At a 5V operation the chip dissipated 250 mW.

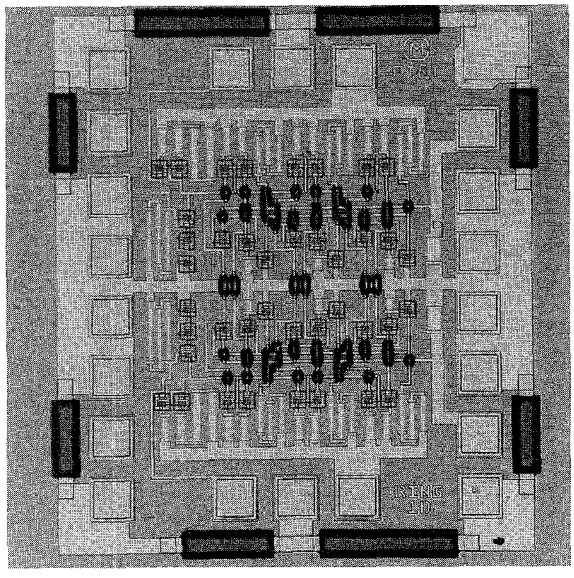

Figure 5: 26 GHz chip photograph.

CONCLUSIONS

Both 10 and 26 GHz differential oscillators have been demonstrated using InP HBT technology. Each have used a 3 stage ring oscillator architecture for the fundamental core. The 26 GHz oscillator has a patented summed output providing a theoretical 1 delay design. The phase noise for the 10 and 26 GHz oscillators was -83 dBc/Hz and -70 dBc/Hz respectively for a 100 kHz offset and -97 dBc/Hz and -85 dBc/Hz for 1 MHz offset. The circuits dissipate 250 mW from a single 5V supply and have a chip size of 870X975 μm^2.

ACKNOWLEDGMENTS

The authors would like to thank D. V. Lang, N. G. Ziesse, and W. J. Clifford for their continued support and encouragement.

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